AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0032], on page 10, with the following new paragraph:

[0032] If the lock register 80 is not in use, the switch 65 issues a retry command in step 640, which is performed similarly to step 625. Then, in step 645, the switch 65 sets the lock flag 61 and sets the request data Rd1 70 into the field 62 of the lock register 80, and also sets the request data Rd2 75 into the field 67 of the lock register 85, then broadcasts the lock register 80 information to all memory controllers 21, 36, and 97. In step 650, node 0, node 1, node 2, and node 3 flush all request queues and signal their respective processors to retry all requests except write-backs to the soon-to-be locked address. Following the sequence shown in Figures 2-3, the memory controllers 21, 36, and 97 update their shadow lock registers 60a, 60b, and 60c (and 63a, 63b, and 63c if a split lock was used in step 655), granting exclusive access to the memory location to processor 20a. The memory controller 21 then waits for the lock request to be retried by processor 20a, possibly performing other memory accesses or other actions in the interim. ~~When~~ Then the processor 20a ~~retires~~ retries the lock request in step 660, returning to step 610. In step 660, the processor 20a reasserts the lock request and again the control is transferred to step 610.